LISTING OF CLAIMS:

1 - 8. (Canceled)

9. (Previously presented): The method according to claim 13 including depositing the layer of conductive material to a thickness which is less than that of the gate.

10. (Currently amended): The method according to claim [[8]] 13 including depositing the layer of conductive material in a non-conformal layer.

11. (Currently amended): The method according to claim [[8]] 13 including depositing the layer of conductive material by sputtering.

12. (Currently amended): The method according to claim [[8]] 13 including depositing said layer of conductive material as a metallic layer.

13. (Currently amended): A method of fabricating a polycrystalline silicon channel TFT with a gate overlying the channel, having an upstanding gate side wall, the method comprising the steps of:

(a) providing a gate separated from a polycrystalline silicon layer by an insulating layer:

(b) implanting a dopant into the polycrystalline silicon layer using the gate as a mask;

(c) forming a spacer after step (b) adjacent to the gate that comprises a conductive region which overlies the polycrystalline silicon layer and extends along the gate side wall, comprising

depositing a layer of conductive material over the polycrystalline silicon layer and the gate, and selectively etching the deposited layer of conductive material to form the spacer with a first portion overlying the polycrystalline silicon layer and a second portion extending along on the side wall of the gate, wherein the selective etching of the conductive layer is carried out by forming a fillet over the first portion thereof, and selectively etching the conductive layer where not protected by the fillet; and

(d) implanting a dopant into the polycrystalline silicon layer using the gate and the spacer as a mask to form a source or drain region, such that the spacer overlies an LDD region in the polycrystalline silicon layer between the source or drain region and the channel.

14. (Previously presented): The method according to claim 13 including depositing a further layer on said conductive layer, and selectively etching the further layer to form the fillet therefrom.

15. (Previously presented): The method according to claim 14 including depositing the further layer as a conformal layer.

16. (Currently amended): ~~The method according to claim 14 including~~

A method of fabricating a polycrystalline silicon channel TFT with a gate overlying the channel, having an upstanding gate side wall, the method comprising the steps of:

(a) providing a gate separated from a polycrystalline silicon layer by an insulating layer;

(b) implanting a dopant into the polycrystalline silicon layer using the gate as a mask;

(c) forming a spacer after step (b) adjacent to the gate that comprises a conductive region which overlies the polycrystalline silicon layer and extends along the gate side wall, comprising depositing a layer of conductive material over the polycrystalline silicon layer and the gate, and selectively etching the deposited layer of conductive material to form the spacer with a first portion overlying the polycrystalline silicon layer and a second portion extending along on the side wall of the gate, wherein the selective etching of the conductive layer is carried out by forming a fillet over the first portion thereof, and selectively etching the conductive layer where not protected by the fillet, wherein the fillet is formed by depositing ~~the~~ a further layer as a Si containing layer on said conductive layer, and selectively etching the further layer to form the fillet therefrom; and

(d) implanting a dopant into the polycrystalline silicon layer using the gate and the spacer as a mask to form a source or drain region, such that the spacer overlies an LDD region in the polycrystalline silicon layer between the source or drain region and the channel.

17. (Previously presented): ~~The method according to claim 14 including~~

A method of fabricating a polycrystalline silicon channel TFT with a gate overlying the channel, having an upstanding gate side wall, the method comprising the steps of:

(a) providing a gate separated from a polycrystalline silicon layer by an insulating layer;

(b) implanting a dopant into the polycrystalline silicon layer using the gate as a mask;

(c) forming a spacer after step (b) adjacent to the gate that comprises a conductive region which overlies the polycrystalline silicon layer and extends along the gate side wall, comprising depositing a layer of conductive material over the polycrystalline silicon layer and the gate, and selectively etching the deposited layer of conductive material to form the spacer with a first

portion overlying the polycrystalline silicon layer and a second portion extending along on the side wall of the gate, wherein the selective etching of the conductive layer is carried out by forming a fillet over the first portion thereof, and selectively etching the conductive layer where not protected by the fillet wherein the fillet is formed by depositing ~~the~~ a further layer by CVD on said conductive layer, and selectively etching the further layer to form the fillet therefrom; and

(d) implanting a dopant into the polycrystalline silicon layer using the gate and the spacer as a mask to form a source or drain region, such that the spacer overlies an LDD region in the polycrystalline silicon layer between the source or drain region and the channel.

18-19. (Canceled)

20. (New): The method according to claim 16 including depositing the layer of conductive material to a thickness which is less than that of the gate.

21. (New): The method according to claim 16 including depositing the layer of conductive material in a non-conformal layer.

22. (New): The method according to claim 16 including depositing the layer of conductive material by sputtering.

23. (New): The method according to claim 16 including depositing the further layer as a conformal layer.

24. (New): The method according to claim 17 including depositing the layer of conductive material to a thickness which is less than that of the gate.

25. (New): The method according to claim 17 including depositing the layer of conductive material in a non-conformal layer.

26. (New): The method according to claim 17 including depositing the layer of conductive material by sputtering.

27. (New): The method according to claim 17 including depositing the further layer as a conformal layer.

28. (New): The method according to claim 13, further comprising the step of forming additional layers over the fillet after step (d), so that the fillet remains within the TFT finally formed.

29. (New): The method according to claim 13, further comprising the step of retaining the fillet over the spacer after step (d), so that the fillet remains within the TFT finally formed.

30. (New): The method according to claim 13, wherein the fillet remains over the spacer after step (d) and within the TFT finally formed.